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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,044	07/15/2003	Srivatsan D.	1-4-2-1-3	7525

7590 02/14/2007
Ryan, Mason & Lewis, LLP
90 Forest Avenue
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EXAMINER

SINKANTARAKORN, PAWARIS

ART UNIT	PAPER NUMBER
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2609

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,044	D. ET AL.	
	Examiner	Art Unit	
	Pawaris Sinkantarakorn	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 14-19 is/are rejected.
- 7) ☒ Claim(s) 12 and 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/3/2003</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claim 12 is objected to because the second occurrence of "associated output interface" seems to refer to "associated output interface previously recited in claim 1 line4, if this is true, it is suggested to change the second "associated output interface" to ---the associated output interface---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For claim 9 line 1, the recitation of "the plurality of sequencing processes" has no antecedent basis.

For claim 16 line 1, the recitation of "the software traffic generator" has no antecedent basis.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 19 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 19 claims "an article of manufacture comprising a storage medium." The claimed subject matter is non-statutory functional descriptive material as stated in the MPEP 2106 Patentable Subject Matter. It is suggested that the applicant rewrite claim 8 in terms of "a computer readable medium, stored with, embodied with, or encoded with a computer program or computer executable instructions."

Claim Rejections - 35 USC § 103

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Art Unit: 2609

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

NOTE: the term "adaptable for" in claim 7 line 3 is not considered a positive claimed limitation; therefore, the limitation following the term is not considered. See MPEP 2111.04.

Claims 1-5, 7, 10-11 and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beanland (US 6,028,847).

For claims 1-5, 7, 10-11, and 14-19, Beanland discloses a method of generating data traffic in a traffic generator (see column 5 lines 66-67 and column 6 lines 1-3), the method comprising the steps of:

generating a plurality of traffic flows (see column 6 lines 39-41); and

associating each of the traffic flows with at least one of a plurality of output interfaces of the traffic generator (see column 7 lines 33-38);

wherein at least one of the traffic flows is generated based on user selection (see column 4 lines 54-58) of at least one of a protocol encapsulation (see column 4 lines 51), a traffic model (see column 3 lines 59-61), and a packet payload description (see column 4 lines 59-64);

wherein the output interfaces are associated with an output interface bus of the traffic generator (see column 4 lines 46-49);

wherein the output interface bus is implemented as a software module representative of one or more physical connections (see column 3 lines 19-21);

wherein each of the plurality of traffic flows maps to one of the output interfaces of the traffic generator (see column 7 lines 33-38) and to an input interface of the traffic generator (see column 3 lines 65-66);

wherein the traffic generator comprises a pattern generator having a plurality of user-selectable pattern generation processes associated therewith (see column 3 lines 19-27);

wherein information characterizing one or more of the traffic flows is stored as a traffic file in a memory associated with the traffic generator (see column 4 lines 66-67);

wherein the traffic file is represented as a string which includes a global header followed by one or more frames each having an associated frame header (see column 2 lines 66-67 and column 3 lines 1-2);

wherein the traffic generator comprises a hardware traffic generator (see column 3 lines 58-62);

wherein the traffic generator comprises a software traffic generator (see column 3 lines 19-21);

wherein the software traffic generator comprises an element of a software-based development tool for simulating the operation of an electronic system (see column 3 lines 19-21) .

An apparatus for generating data traffic, the apparatus comprising an information processing device having a processor (see column 3 line 19) and a memory (see

Art Unit: 2609

column 4 lines 66-67), the information processing device implementing a traffic generator operative (see column 5 lines 66-67 and column 6 lines 1-3):

- to generate a plurality of traffic flows (see column 6 lines 39-41); and
- to associate each of the traffic flows with at least one of a plurality of output interfaces of the traffic generator (see column 7 lines 33-38).

An article of manufacture comprising a storage medium containing one or more software programs for use in generating data traffic in a traffic generator (see column 5 lines 66-67 and column 6 lines 1-3), wherein the one or more software programs when executed implement the steps of:

- generating a plurality of traffic flows (see column 6 lines 39-41); and
- associating each of the traffic flows with at least one of a plurality of output interfaces of the traffic generator (see column 7 lines 33-38).

Beanland discloses all the subject matter of the claimed invention except the method of implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces and method of generating data traffic wherein the traffic generator is implemented primarily in software and is configured to generate data traffic files that are utilizable in another traffic generator implemented primarily in hardware. However, it is well known to the person of ordinary skill in the art.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement a method of implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces and a method of generating data traffic wherein the traffic generator is implemented primarily in software

and is configured to generate data traffic files that are utilizable in another traffic generator implemented primarily in hardware.

The method for implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces can be implemented by assigning a sequence number field in each of the data packets so that the traffic flows can be identified at the receiving terminal. The method for generating data traffic wherein the traffic generator is implemented primarily in software and is configured to generate data traffic files that are utilizable in another traffic generator implemented primarily in hardware can be implemented by adding a processor in a traffic generator implemented primarily in hardware to read the data traffic files generated by a software traffic generator and then generate traffic flows accordingly.

The motivation for implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces is that it reduces the number of output interfaces needed in a traffic generator, which leads to the reduction in hardware costs. The motivation for implementing a method for generating data traffic wherein the traffic generator is implemented primarily in software and is configured to generate data traffic files that are utilizable in another traffic generator implemented primarily in hardware is that it allows a system to have both software and hardware traffic generator, which makes the system more flexible.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2609

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Beanland in view of Dieterich et al. (US 6,208,643).

For claim 6, Beanland discloses a method of generating data traffic described in paragraph 6 of this office action except the method of generating packets using a timestamp table. The invention of Dieterich et al. from the same or similar fields of endeavor teach a method of constructing a timestamp table in the memory of a processor.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement the method of generating packets using a timestamp table.

The method of generating packets using a timestamp table can be implemented by implementing a clock to keep track of the time of arrival of each input packets and store the data in a memory of a processor.

The motivation for implementing a method of generating packets using a timestamp table is that it enables synchronization of the system.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2609

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beanland in view of McNamara (US 6,262,976).

For claims 8-9, Beanland discloses a method of generating data traffic described in paragraph 6 of this office action except the method: wherein the traffic generator comprises a sequencer having a plurality of user-selectable sequencing processes associated therewith, a given one of the sequencing processes specifying an order of selection of items from a configuration list; wherein the plurality of sequencing processes comprises a group sequencer which provides a correlative mapping between two or more configuration lists and their associated parameters. The invention of McNamara from the same or similar fields of endeavor teaches different types of sequencing processes (see column 13 lines 19-30).

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement the method, wherein the traffic generator comprises a sequencer having a plurality of user-selectable sequencing processes associated therewith, a given one of the sequencing processes specifying an order of selection of items from a configuration list; wherein the plurality of sequencing processes comprises a group sequencer which provides a correlative mapping between two or more configuration lists and their associated parameters.

The method, wherein the traffic generator comprises a sequencer having a plurality of user-selectable sequencing processes associated therewith, a given one of the sequencing processes specifying an order of selection of items from a configuration

Art Unit: 2609

list; wherein the plurality of sequencing processes comprises a group sequencer which provides a correlative mapping between two or more configuration lists and their associated parameters can be implemented/modified by adding a sequencer in the processor of the system.

The motivation for implementing the method, wherein the traffic generator comprises a sequencer having a plurality of user-selectable sequencing processes associated therewith, a given one of the sequencing processes specifying an order of selection of items from a configuration list; wherein the plurality of sequencing processes comprises a group sequencer which provides a correlative mapping between two or more configuration lists and their associated parameters is that it enables a user to have more control over traffic generation by allowing the user to select his/her own sequencing processes.

Allowable Subject Matter

9. Claims 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if rewritten to overcome the objection, set forth in this office action.

For claims 12-13, the prior art fails to teach the clock speed field indicating a clock speed of an associated output interface in the global header, and timing field indicating a time gap in clock cycles between the corresponding frame and a previous frame in the frame header.

Art Unit: 2609

Conclusion

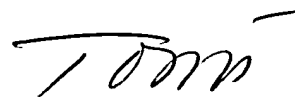
10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jones et al. (US 6,067,286) and Blair (US 6,778,495) are cited to show systems that are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pawaris Sinkantarakorn whose telephone number is 571-270-1424. The examiner can normally be reached on Monday-Thursday 7:30am-4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton can be reached on 571-272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PS



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SUPERVISORY PATENT EXAMINER